forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode;

connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor; and

F1

incorporating said multi-region planar thyristor in a memory device, said memory device adapted to store information using said latchup of said multi-region planar thyristor.

(sub G2)

55. (Once Amended) A method of forming a device for storing information as one of at least two possible stable current states, the method comprising the following steps:

F2

providing a semiconductor substrate;

providing doped silicon regions to form a multi-region planar thyristor having at least four regions;

forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode, said gate adapted to receive a voltage for producing latch-up in said multi-region planar thyristor ;and

incorporating said multi-region planar thyristor in a memory device, said memory device adapted to store information using said latchup of said multi-region planar thyristor.